H R D 16

High-Speed-RAM-DSR

Memory-Board

system 99 user-group 1998

HARDWARE INSTALLATION MANUAL

(10/1998)

1 FOREWORD

Here you go with the sixth **P-BOX-Board** of the system 99 user-group! Enjoy yourself!
History:

1990: BwG-Disk-Controller with RTC. Because ”w” had fooled us, unfortunately never with an own DSR but instead Atronic compatible. Production volume over 80! Was available until 1993.
New and last series allready made! With our first own DSR now!

1994: EVPC-80 column board with VGA-DAC. Production volume 50, still some available.
New series possible!

1995: HSGPL-Super-GROM/GRAM-Board with new GROM-0. Up to 2MB FEPROM, in-system-programmable. Production volume 50, still available.

1996: SGCPU-The TI 99/4P with up to 1MB-AEMS-compatible RAM and more. Production volume 30, still available.

1997: ASCSI licenced Upgrade of the WHT-SCSI-Board from the states.
still available.

1998: HRD16-High-Speed-RAM-DSR in 16 bit mode for all TI and SGCPU computers
Still available, but only 20 pieces were produced.

2 INTRODUCTION

This manual covers the installation of the HRD16-Board into the P-Box and their use and configuration together with the 99/4A-Computer-System. It describes NOT the function of the software or the handling of the Disk-Manager-Software. This document is ONLY intended to describe the installation of the peripheral board.

3 INSTALLATION

The HRD16-Memory Board is a peripheral board in standard format for use with the Texas Instruments 99/4A or TI99/4P (”SGCPU”). To be able to use this board you MUST have the following configuration:
TI 99/4a console, monitor, 32K-memory expansion, P-box

OR
SGCPU, EVPC, HSGPL, monitor, P-box
Before the installation be sure that all components are totally switched off and the power cords are disconnected.

4 SETTING OF DIP-SWITCHES AND JUMPERS

The HRD16-Board contains one DIP-switch and several jumpers for configuration of the hardware. They are placed on the main PCB and are named S1, JP1, JP2, JP3, JP4 and JU1, JU2, JU3. S1 defines the CRU address of the PCB, the jumpers are used to control different extension versions and operation modes.

4.1 CONFIGURATION OF DIP-SWITCH S1

S1 defines the CRU address (Communications Register Unit) of the PCB. The following table shows all possible settings for the HRD16. Included in the table are also all the other possible peripherals which might occupy the same CRU addresses. For proper function it is very important for the PCB that the address space is only occupied by the HRD16-board. If you have installed any of the listed boards you have to configure the HRD16 for an address which is not already used. The pre-configured address for the HRD16-board is >1200. A possible alternative is >1000, which allows the board to catch (and therefore emulate) all device names during the ”DSRSCAN”.

	A4	***A5***	***A6***	***A7***	***=processor-adresses***
CRU	**DIP 1**	**DIP 2**	**DIP 3**	**DIP 4**	**released hardware**
>1000	ON	ON	ON	ON	HFDC, HORIZON’s
>1100	ON	ON	ON	OFF	All Diskcontrollers,HFDC
>1200	ON	ON	OFF	ON	
>1300	ON	ON	OFF	OFF	RS232 Nr.1
>1400	ON	OFF	ON	ON	EVPC 80-column-card
>1500	ON	OFF	ON	OFF	RS232 Nr.2
>1600	ON	OFF	OFF	ON	
>1700	ON	OFF	OFF	OFF	PGRAM(+) ASCSI, SCSI
>1800	OFF	ON	ON	ON	TI-Thermoprinter
>1900	OFF	ON	ON	OFF	
>1A00	OFF	ON	OFF	ON	
>1B00	OFF	ON	OFF	OFF	**HSGPL, nothing else!**
>1C00	OFF	OFF	ON	ON	
>1D00	OFF	OFF	ON	OFF	IEEE8-Controller
>1E00	OFF	OFF	OFF	ON	AMS/AEMS/SGCPU
>1F00	OFF	OFF	OFF	OFF	P-Code-card

The HRD16-board will also work together with several other HRD's:

There are too many possible combinations to list everything. If you are therefore not sure how to configure the CRU address for your system, you may contact us.

4.2 CONFIGURATION OF JUMPER JP1, JP2

Those two jumpers define the operation mode as well as the installed amount of memory. Jumper JP1 defines the memory size installed and therefore also the correct chip select signals for the RAM-chips on the PCB. It is marked with *"**SIZE**"* on the PCB using silk screen printing.

JP1	**used RAM-size:**
closed	512K*8 (628512)
open	128K*8 (628128)

Jumper JP2 defines the method of memory access. Memory is accessed in 8-bit mode (together with all TI99's) or in 16-bit mode (only with SGCPU). It is marked with *"**WIDTH**"* on the PCB.

JP2	**selected Buswidth:**
closed	16-bit
open	8-bit

Jumper JP4 is designed for switching the board off if necessary. Instead of the Jumper a switch might be installed. This makes it possible to disable the HRD16 without removing the board. It is marked with *"**DISABLE**"* on the PCB.

JP4	**selected action:**
closed	card disabled
open	card enabled

Jumper JP5 disconnects the battery power supply from the memory chips if necessary. It is normally connected and the memory chips are supplied by the installed lithium battery with power while the P-box is switched off (for RAMDISK-use). It is marked with *"**BATTERY**"* on the PCB.

5 WIRING

The HRD16-board is optionally delivered with a link cable for connecting the High-order-Bus with the SGCPU. This cable is needed to connect additionally the 8 higher data bits parallel to the lower 8 data bits of the data bus. It lies above the PCBs and is connected 1:1 with the SGCPU (connector is coded). To keep it as short as possible be sure to place both boards as close together as possible. It is also possible to attach more than one HRD16s to one SGCPU. In this case you have to mention it before ordering, because the additional connectors have to be mounted on the cable.

6 ADDITIONAL INFORMATION

Due to the chosen board design and the involved 16 bit design it is necessary to always install the memory chips in pairs. That means either 2, 4, or 6 chips. The other memory chips are already placed on the PCB. You have to start with the pair U26/U31, follow on with U27/U28 and end up with U29/U30. This is the only possible way to ensure a memory decoding without gaps. As mentioned above, this way of installation is also necessary for 8-bit use, because the board internally always works in 16-bit mode.

7 POWER SUPPLY

The HRD16 supplies itself totally from the built-in power supply of the P-box. The design allows, which is different from other HRD's, to shorten the voltage regulator, for example if a regulated PC power supply is used. The functionality of the battery backup is still guaranteed! The lithium battery is mounted outside of the P-pox and MUST NOT be shortened, DANGER OF EXPLOSION! For safety reasons a resistor is on the board which reduces the current if a RAM or a capacitor is defective. But this resistor does not help if the HRD16 board is laid onto a metal surface, because the resistor itself would be shortened in this case! Please put the HRD16 board always in or on ***antistatic, but not conductive*** wrapping / desk pads. Otherwise the lithium battery will be discharged! We propose those black antistatic-bags, which are labelled as that or paper of a simple newspaper, but not of a glossy magazine.

8 SPECIAL SETTINGS

8.1 Usage of EPROM's for the lower 6Kb of the DSR

Instead of RAM you may put EPROMs into the sockets U32/U33 (EPROM-Type 2732). In this case you must necessarily use the following settings, otherwise the lithium battery will be discharged very soon:

Unfortunately you have to change three jumpers, because the power supply of both EPROMs has to be changed from backuped to normal and because both chip-select signals must be changed from backuped to normal.

The setting of the jumpers JU1, JU2 and JU3 is the following:
Pin numbering is like pin 1 is the upper pin, pin 2 the middle and pin 3 the lowest one (as can be seen when P-box is opened and board plugged in). There are only two different allowed combinations of jumper settings as described below.

8.1.1 Variation 1: Usage with RAM's of Type 62256 (32K*8)

JU1: Jumper on Pin 1-2
JU2: Jumper on Pin 2-3
JU3: Jumper on Pin 1-2

8.1.2 Variation 2: Usage with EPROM's of Type 2732 (4K*8)

JU1: Jumper on Pin 2-3
JU2: Jumper on Pin 1-2
JU3: Jumper on Pin 2-3

All the other possible combinations will cause malfunction or will discharge the lithium battery.

8.2 Usage of Memories with Slim-line-Packaging

It is likely that in the future no more (0,6 inch) DIL-RAM's will be available. Therefore the Layout of the board is already prepared for different kinds of memory packages. An exception from this are the sockets U32/U33, because the system 99 user-group has a lot of memories of type 2732 as well as 62256 on stock.
Advice: when supplementing the board with small memory chips (0,3 inch) be aware to place them **on the right pair of pads**, because the middle row of pads is connected to the left row. Plugging the memories into the left row will not cause any damage, the memory will just not work.

8.3 Memory-Areas:

adress-space	function:
>4000-57FF	base-DSR, 6KB
>5800-5FFF	Paged-DSR, each 2K-“RACK“. multiple-banked via CRU-bits.

8.4 CRU-bits during Write Access:

offset:	description:
>00	DSR-Enable for the whole card
>01	lowest Paging bit
>02	Paging bit
>03	Paging bit
>04	Paging bit
>05	Paging bit
>06	Paging bit
>07	Paging bit
>08	Paging bit
>09	Paging bit
>0A	Paging bit
>0B	highest Paging bit

Responding to the installed memory each 2KB-Block is selected by calculating the address with the formula:

CRU-DATA = (2*Rack-Number)+1
f.e. Rack-Number 5 results in CRU-DATA >000B

This result CRU-DATA must be written with the LDCR-command to the CRU-BASIS address. ”1” is always added, because >00 is used to enable the HRD16-board. You could avoid this by always accessing the single CRU-bits with SBO/SBZ-commands, but this would be far too much trouble.

8.5 CRU-bits during Read Access:

As all the newer snug-boards this board has an implemented CRU-identifier. It returns on CRU-offset >20 the code **>A561** (in this first revision).

The CRU-identifier is composed of the following information

>A5 >61	1010 0101	011	00001
Ident-code:	allways: >A5		
	card-number:	*001 for ASCSI2* *010 for SPVMC* 011 for HRD16	
		card-revision:	hier #1 ***[the ASCSI2 has revision-Nr. #2]***

To save money decoding is not complete, so you will get this information also on multiples of this offset (f.e.: >00, >20, >40...).

Advice:
Because for the revision numbers 5 bit are not really necessary, at least the first 2-bit of this block are available for future use.

9 Parts List

This list is only meant for acquiring spare parts for repair and/or upgrade of the board.

count	designator	description	comment
1	BT1	3,6V Litium-cell	size AA
22	C3,C4,C5,C6,C7,C8,C9,C11 ,C12,C15,C16,C22,C23,C24, C26,C27,C28,C29,C30,C31, C32,C33	0.1 ceramic or MKT	200MIL-size
1	C1	0.1 MKT	200MIL-size
1	C2	0.22 MKT	200MIL-size
3	C14,C25,C34	10uF/35V ALU	100MIL-size
1	C17	22uF	100MIL-size
1	D1	LED green	in 90° holder
1	D2	FDH300	or similar
1	D3	2V7 Z-diode, 0,5W	
1	J1	BUS	gold-plated
1	JP1	SIZE	jumper-bridge
1	JP2	WIDTH	jumper-bridge
1	JP3	5x2 Flat-Cable-Conn.	16 bit-connec.
1	JP4	DISABLE	jumper-bridge
1	JP5	BATTERY	jumper-bridge
6	JP6,JP7,JP8,JP9,JP10,JP11	16pol Socket-strip	combilayout
1	JU1	TYPE	Jumper 3pol.
1	JU2	TYPE_H	Jumper 3pol.
1	JU3	TYPE_L	Jumper 3pol.
1	Q1	2N2369A	NPN-TTL
1	Q2	2N4033	PNP-switch
1	Q3	BCY59	or similar
1	R32	0R82	shortened
2	R10,R19	100R	
2	R29,R31	150R	
1	R30	470R	
3	R1,R4,R16	1K0	
1	R18	2K2	
4	R17,R21,R22,R24	4K7	
1	R2	6K8	
1	R3	10K	
1	R26	SIL-R4	4*10K o.sim.

count	designator	description	comment
1	S1	SW DIP-4	
1	U1	7805	on 09/37
1	U2	TL7702	
1	U6	74HCT240	
2	U7,U8	74HCT244	
2	U9,U21	74LS245	
1	U11	74LS125	
1	U20	74HCT245	
1	U23	MACH210-15JC	MACH-HRD
2	U24,U25	74HC138	
6	U26,U27,U28,U29,U30,U31	628512	or 628128
2	U32,U33	62256, RAM 32K*8	or 2732
1	U34	PALCE22V10	HRD_PAL2
1	U2	socket 8-pol	300MIL
1	U11	socket 14-pol	300MIL
2	U24,U25	socket 16-pol	300MIL
6	U6,U7,U8,U9,U20,U21	socket 20-pol	300MIL
1	U34	socket 24-pol	300MIL
2	U32,U33	socket 28-pol	600MIL
6	U26,U27,U28,U29,U30,U31	socket 32-pol	300/600MIL
1	U23	socket 44-pol	PLCC

10 DSR-Loader

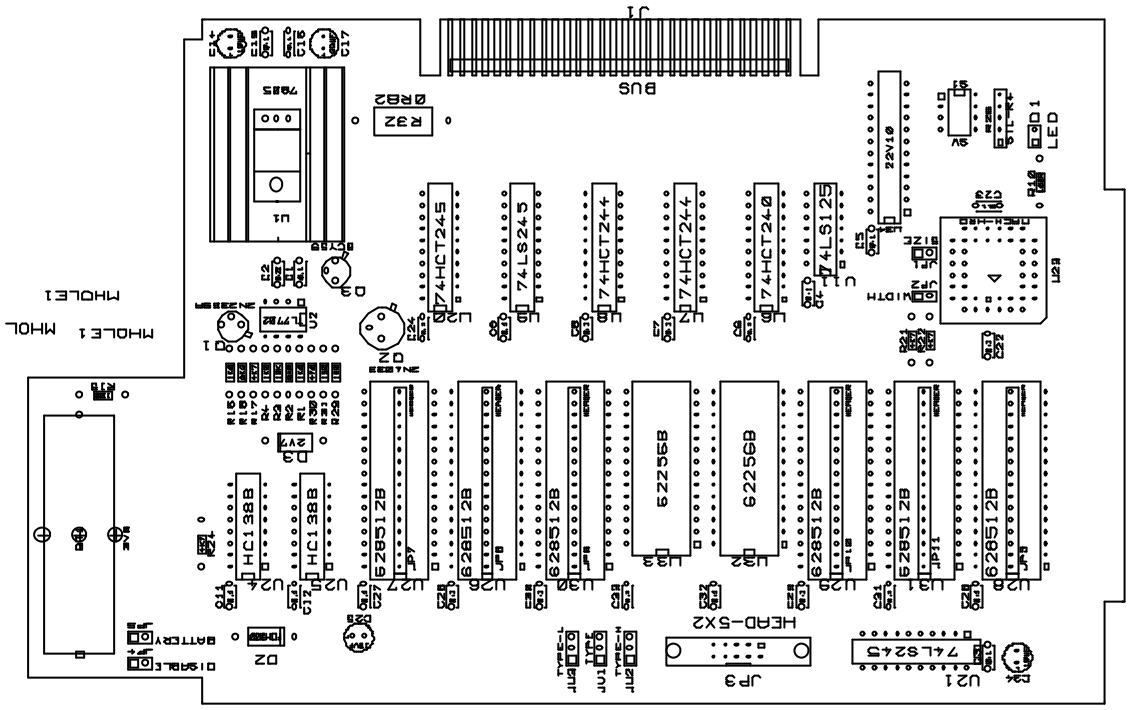
Due to the CRU-identifier it would be possible to access this board with the DSR-Loader, version 2.xx upwards. But at the moment the HRD16 is still not supported.

11 Further Software

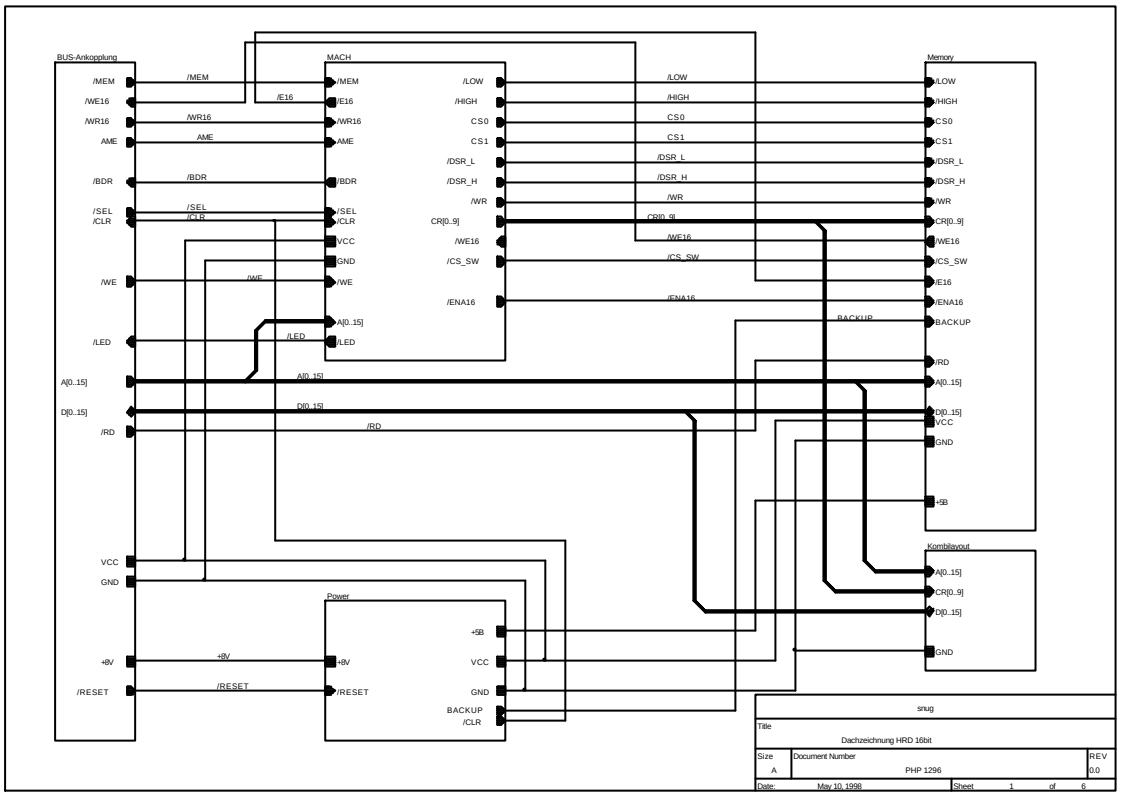
Basically it is possible, after buying a HORIZON-ROS, to use the HRD16 like one. This Operating System is definitely not Freeware and is not distributed by snug. The HRD16 would work like a standard HRD, without the special GENEVE-functionality (RAMBO etc.).

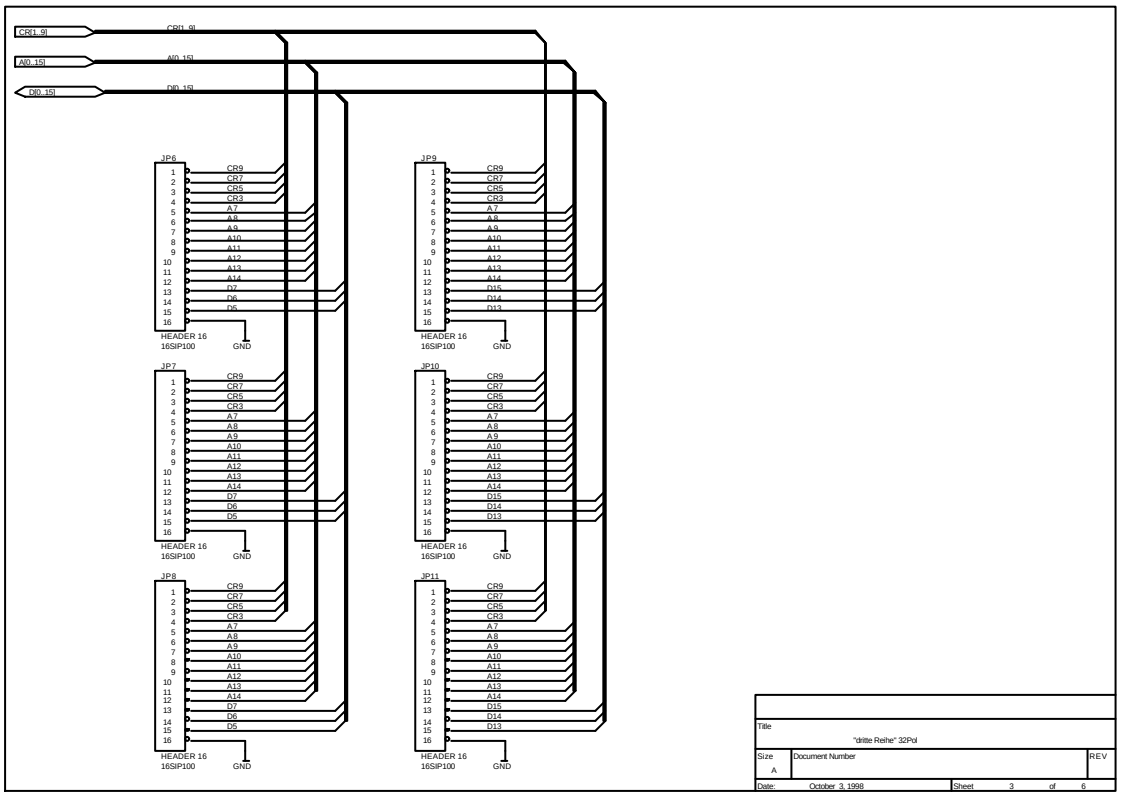
12 Addendum

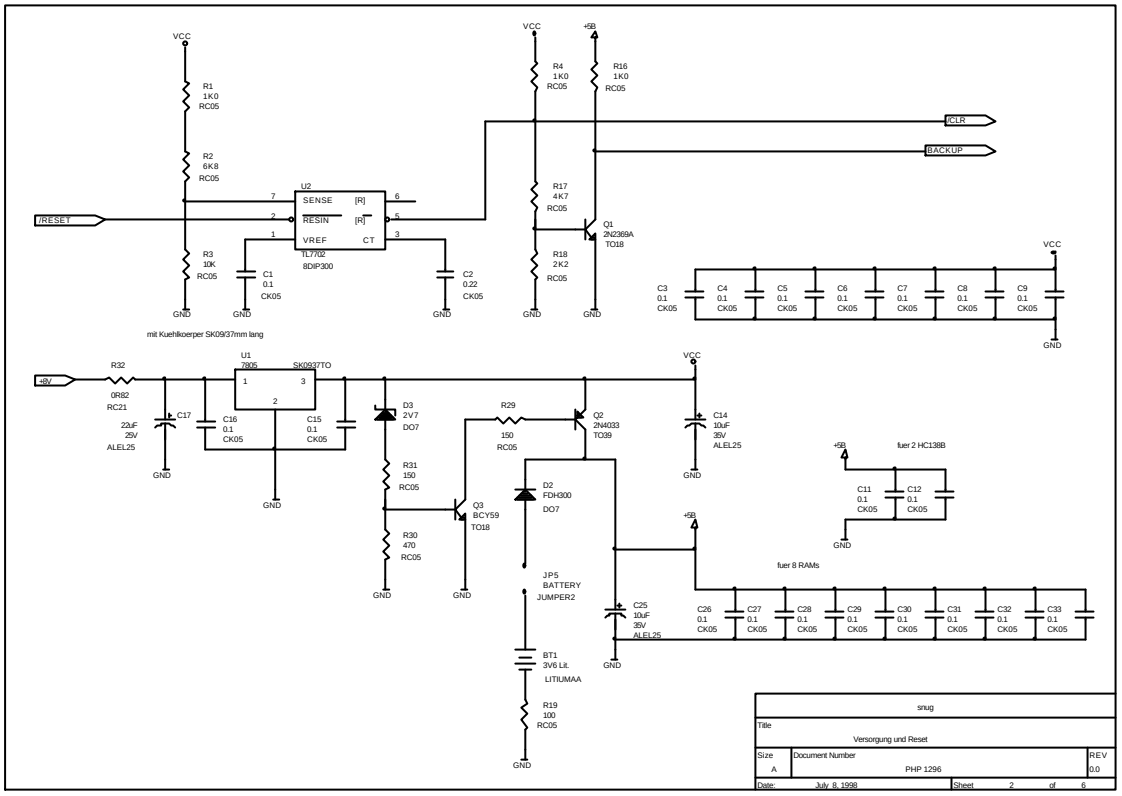
12.1 Component Layout



12.2 Schematic Diagrams



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+5B
R1 1K0 RC05
R2 6K8 RC05
R3 10K RC05
R4 1K0 RC05
R16 1K0 RC05
R17 4K7 RC05
R18 2K2 RC05
U2
SENSE
RESIN
VREF
TL7702
8DIP300
/RESET
/CLR
BACKUP
Q1 2N2369A TO18
C1 0.1 CK05
C2 0.22 CK05
C3 0.1 CK05
C4 0.1 CK05
C5 0.1 CK05
C6 0.1 CK05
C7 0.1 CK05
C8 0.1 CK05
C9 0.1 CK05
GND
mit Kuehlkoerper SK09/37mm lang
U1 7805 SK0927TO
+8V
R32 0R82 RC21
C17 22uF 25V ALEL25
C16 0.1 CK05
C15 0.1 CK05
D3 2V7 DO7
R29 150 RC05
Q2 2N4033 TO39
C14 10uF 35V ALEL25
R31 150 RC05
D2 FDH300 DO7
Q3 BCY59 TO18
R30 470 RC05
JP5 BATTERY JUMPER2
BT1 3V6 Lit. LITIUMAA
R19 100 RC05
fuer 2 HC138B
C11 0.1 CK05
C12 0.1 CK05
fuer 8 RAMs
C25 10uF 35V ALEL25
C26 0.1 CK05
C27 0.1 CK05
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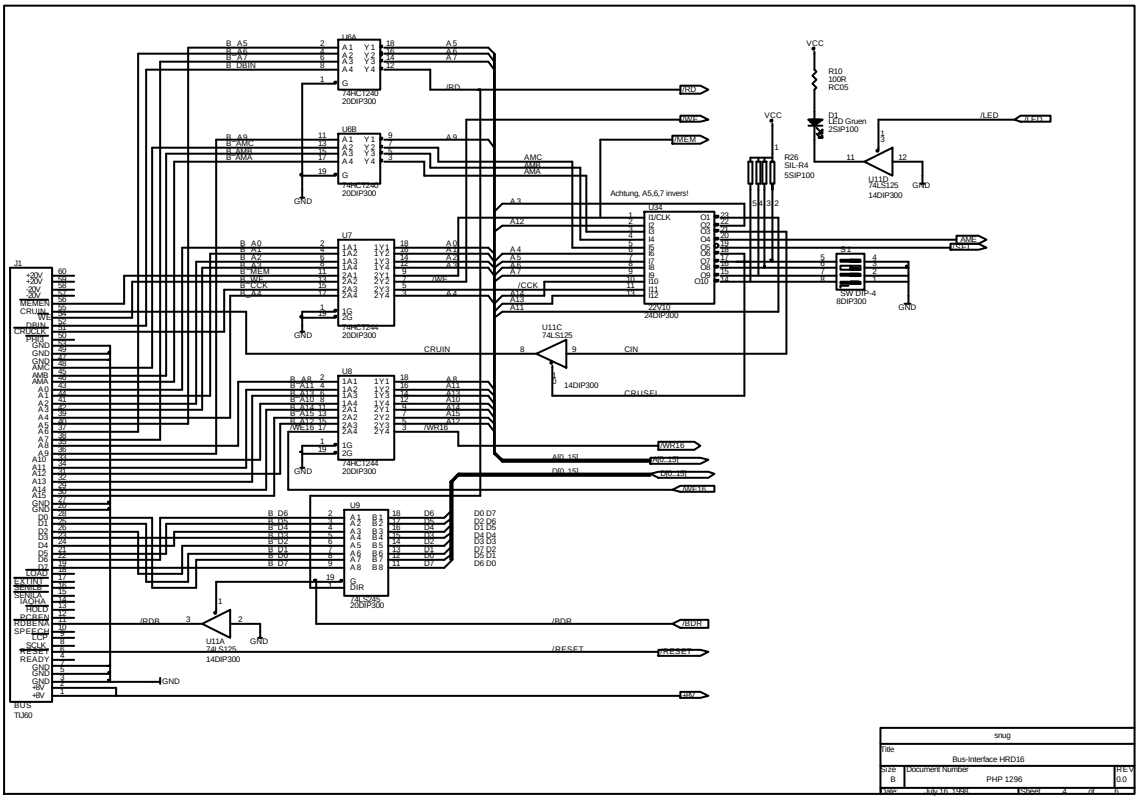
Sheet 2 of 6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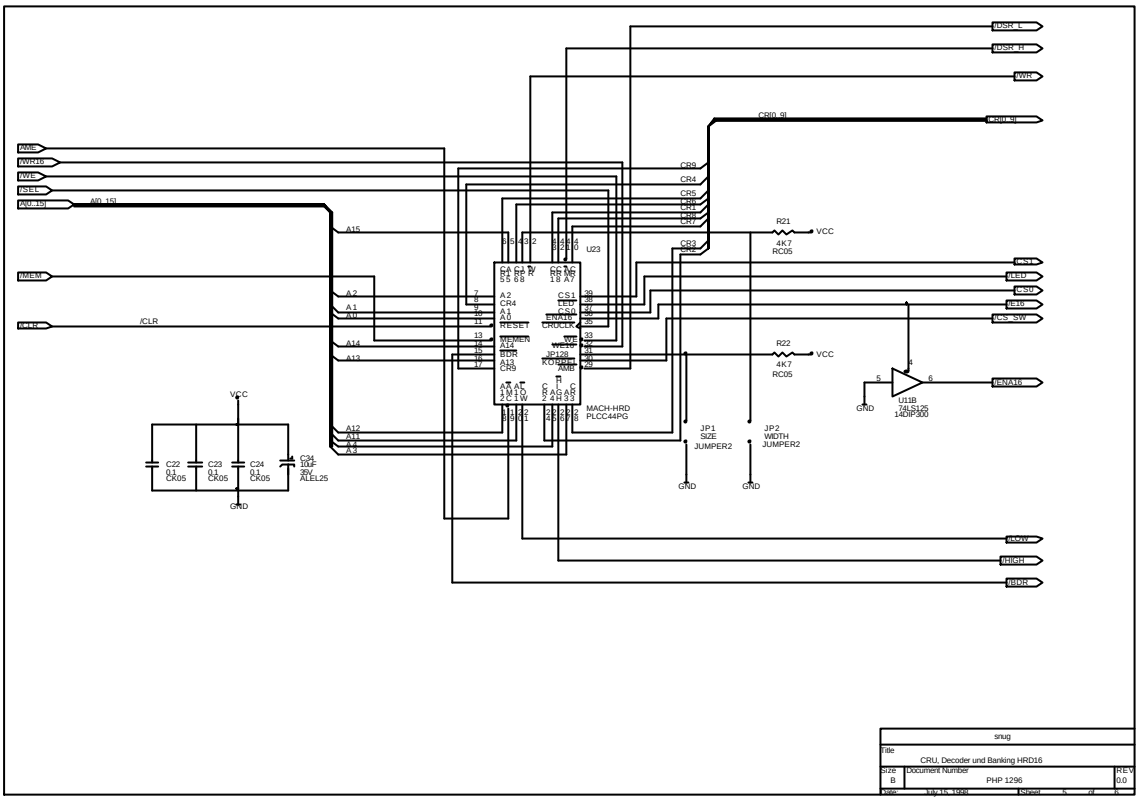
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C23 0.1 CR05
C24 0.1 CR05
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GND
CR9
CR4
CR5
CR6
CR7
CR3
SWE
U23
MACH-HRD PLCC44PG
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RC05
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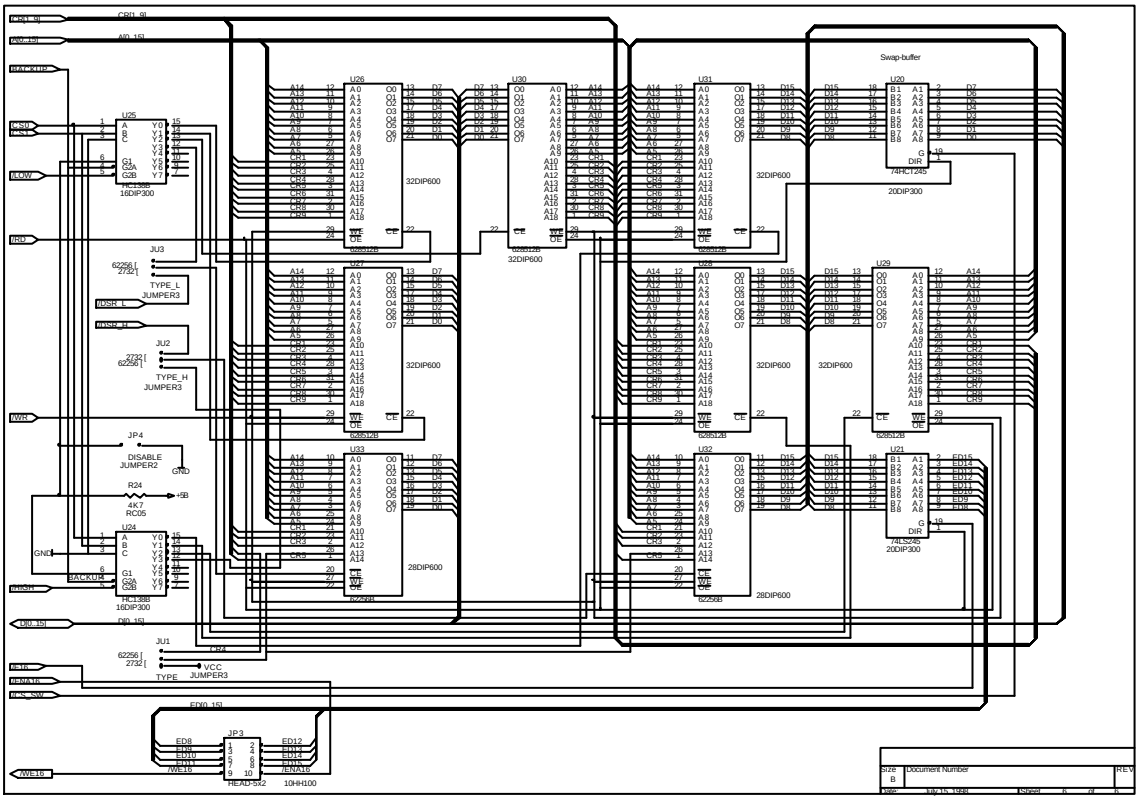
CRU, Decoder und Banking HRD16
PHP 1296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U26
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U30
U31
U20
U21
U22
U33
U24
32DIP600
28DIP600
62512B
62256B
74HCT245
74ALS245
20DIP300
Swap-buffer
JU1
JU2
JU3
TYPE
TYPE_L
TYPE_H
JUMPER3
JP4
DISABLE
JUMPER2
R24
4K7
RC05
+5V
GND
VCC
JP3
HEAD-5X2
10HH100
EDO_15[
ED0_15]

13 Announcement:

Our next Board is ready for layout. It is the Speech-and-Voice-Memory-Board, called **SPVMC**. It is, similar to the HSGPL, a simulation of the speech-ROM's of the TI-Speech-Synthesizer PHP1500 on a PCB, and can also be accessed (like the DSR-ROM) with DSR-Loader 2. Both boards use the same Flash technology. The speech-chip is already on the PCB, nobody has to cannibalize his/her original PHP1500! The speech-ROM-emulation is filled with additional new words I got from America. One part of them is even with a female voice. The program **MEMORY-MANAGER** is already prepared to work together with the SPVMC, but only as version 3.27! We are working on an upgrade for the DSR to access all the additional words with the normal CALL SAY statement!

14 Final Comment

This project again was only made possible with the joint efforts of many individualists:

Michael Becker	idea, hardware-design, PLD-development, documentation
Jürgen Stelter	PCB-design, procurement of parts
Harald Glaab	DSR-loader, CRU-identifier, procurement of PCBs, etc.
Götz Feuerstein	our beta-tester. He for example was the reason for the actual design of the DSR-Loader-2, which is now able to automatically recognize in which board which DSR has to be loaded and for which CRU address this board is actually configured. He is involved in every project from the very beginning.
Francesco L. Lama	my "British-connection", he always tests the English versions. Obviously: Francesco is a teacher in Oxford! He owns all types of snug components and is visiting me in Mannheim at least twice a year on his way to Italy.
Konstantin Socas	the illiterate who tried to translate this document into English. ;-)

Mannheim, im Oktober 1998

Michael

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