

# Hardware-Identification / CRU-ID / PLD-ID

## CRU-ID

To get more exact information about the structure of cards we developed, after ASCSI 2 a hardware-recognition, the so-called **CRU-ID**. Where it was technically feasible, the older cards were also retro-fitted with a **CRU-ID**.

The hardware recognition is always given in the 16 CRU bits from the CRU address >xx20 to >xx3E. The place holder >xx stands for the CRU Basis address of the card, for example >11 for the Disk Controller or >13 for the first RS232.

The CRU-Bit >xx00 (DSR Page Enable) must be read for switching.

For recognition the first 8 bits (CRU >xx30 to >xx3E) are always the same, i.e., 10100101, and set as >A5, so that it can be determined if the card really has a **CRU-ID**.

The danger is that the a card that resides at >xx30 to >xx3E is assigned as >A5, and may have no implemented **CRU-ID** which stands for 256 to 1 and it is too bad that this simple system cannot be improved.

In no case have we found a card with this bit sequence. The only exception is the EVPC with DIP-switches, and can set a combination of >A5 whereby the 8 bit CRU can be recognized (with a valid definition) of >A5A5.

The **CRU-ID** always look like this:

Recognition Byte								CRU	ID
>xx3E	>xx3C	>xx3A	>xx38	>xx36	>xx34	>xx32	>xx30	>xx2E ... >xx28	>xx26 ... >xx20
>A				>5				>0 ... >F	>0 ... >F
1	0	1	0	0	1	0	1	Card	Revision

The **CRU-ID** 00000000 (>00), 10100101(>A5) and 11111111 (>FF) are not intended for use.

Here is a listing of all of the cards with a **CRU-ID**

Card	CRU-ID									
	K	R	Card Recognition				Card Revision			
			>xx2E	>xx2C	>xx2A	>xx28	>xx26	>xx24	>xx22	>xx20
IDENT(*)	1	1	0	0	0	1	0	0	0	1
WHT-SCSI	2	1	0	0	1	0	0	0	0	1
ASCSI 2	2	2	0	0	1	0	0	0	1	0
MDCNT(*)	3	1	0	0	1	1	0	0	0	1
SPVMC	4	1	0	1	0	0	0	0	0	1
HRD 16	6	1	0	1	1	0	0	0	0	1
BwG-2(*)	8	2	1	0	0	0	0	0	1	0
HSGPL	A	1	1	0	1	0	0	0	0	1
EVPC 2	C	2	1	1	0	0	0	0	1	0
HRPIC(*)	E	1	1	1	1	0	0	0	0	1

\* In the table, cards are listed that are in the planning stage for which a CRU-ID has already been assigned.

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### PLD-ID

Individual cards with a **CRU-ID** assigned also have a **PLD-ID**, which is the internal version number of the PLD..

The **PLD-ID** is like the **CRU-ID** which is also a CRU data value at CRU-address >xx20 ;  
The recognition byte is set to >A5 in this case.

The CRU bit >xx00 (DSR Page Enable) must in contrast with the **CRU-ID** be set.

The LowByte supplies the aforementioned **PLD-ID**, where >00 denotes a Beta version.

The **PLD-ID** is only valid when a **CRU-ID** exists!

Recognition Byte								ID
>xx3E	>xx3C	>xx3A	>xx38	>xx36	>xx34	>xx32	>xx30	>xx2E .... >xx>20
>5				>A				>00 ... >FF
0	1	0	1	1	0	1	0	PLD-ID